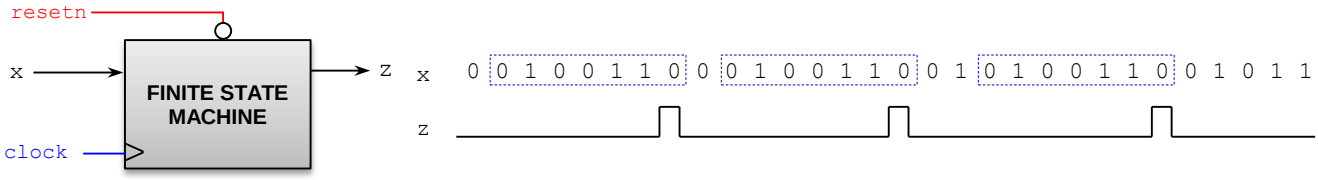
Homework 4

(Due date: March 29th @ 5:30 pm)
Presentation and clarity are very important! Show your procedure!

PROBLEM 1 (23 PTS)

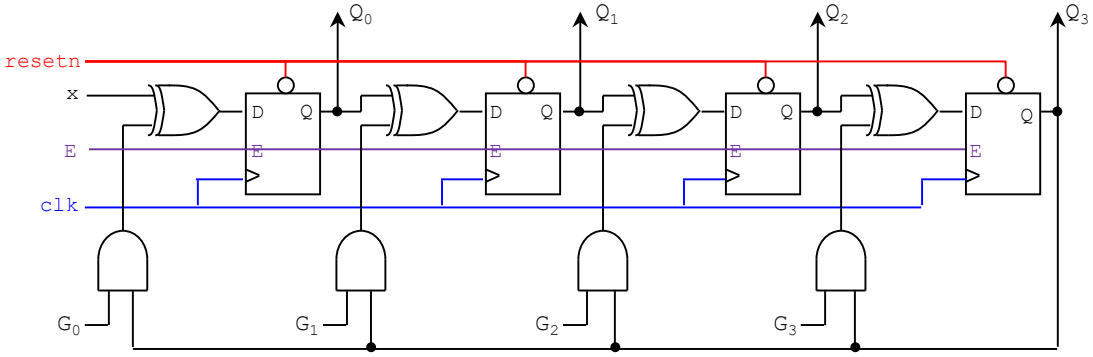
- Sequence Detector: The machine has to generate z=1 when it detects the sequence 0100110. Once the sequence is detected, the circuit looks for a new sequence.

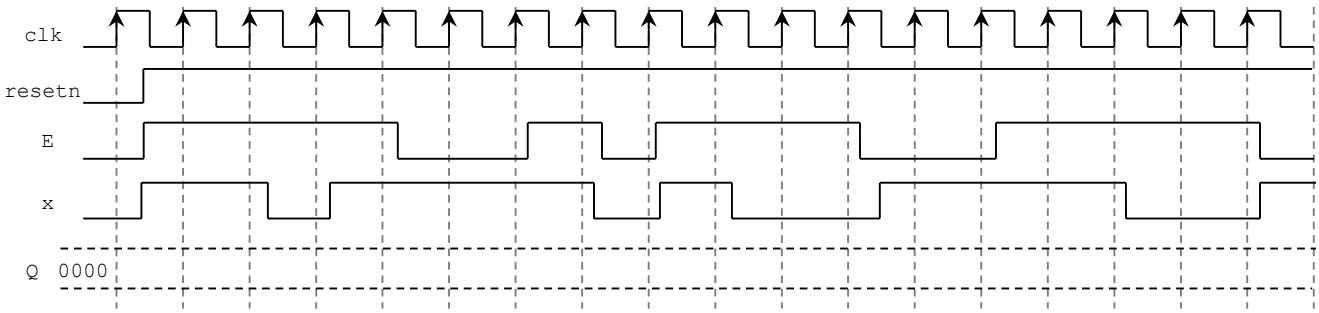


- Draw the State Diagram (any representation), State Table, and Excitation Table. Is this a Mealy or a Moore machine? Why?
- Provide the excitation equations (simplify your circuit using K-maps or the Quine-McCluskey algorithm) (5 pts)
- Sketch the circuit. (3 pts)

PROBLEM 2 (15 PTS)

- Complete the timing diagram of the following circuit. $G = G_3G_2G_1G_0 = 1101$, $Q = Q_3Q_2Q_1Q_0$

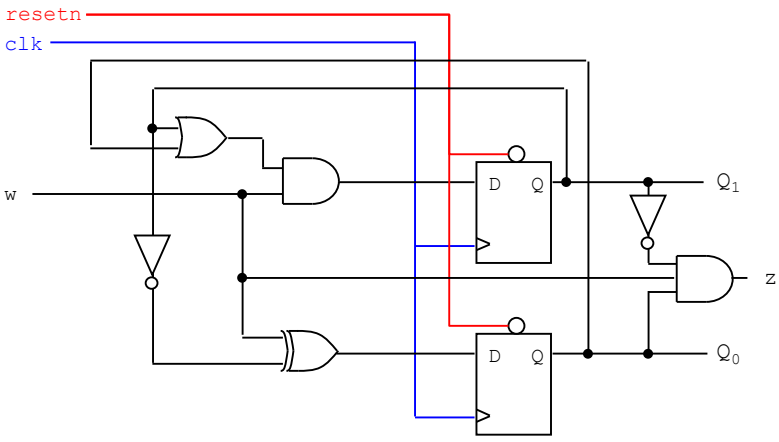




PROBLEM 3 (12 PTS)

- Provide the State Diagram (any representation), the Excitation Table, and the Excitation equations of the following FSM.

  w: input, z: output, Q_1Q_0: state.

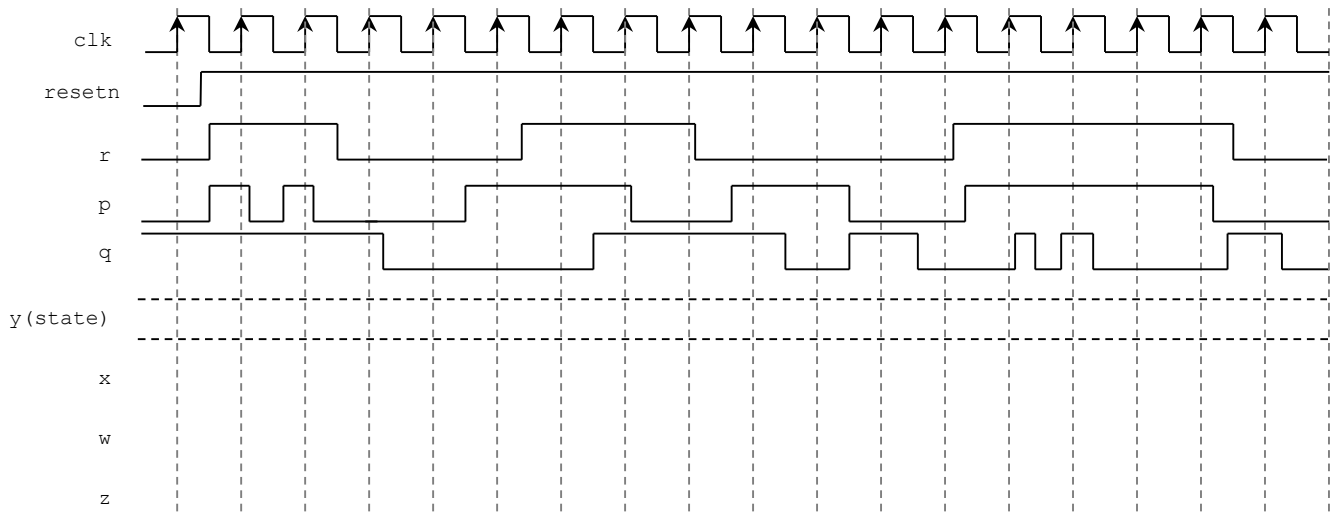


PROBLEM 4 (17 PTS)

- Draw the State Diagram (in ASM form) of the FSM whose VHDL description in shown below. Is it a Mealy or a Moore FSM?
- Complete the Timing Diagram.

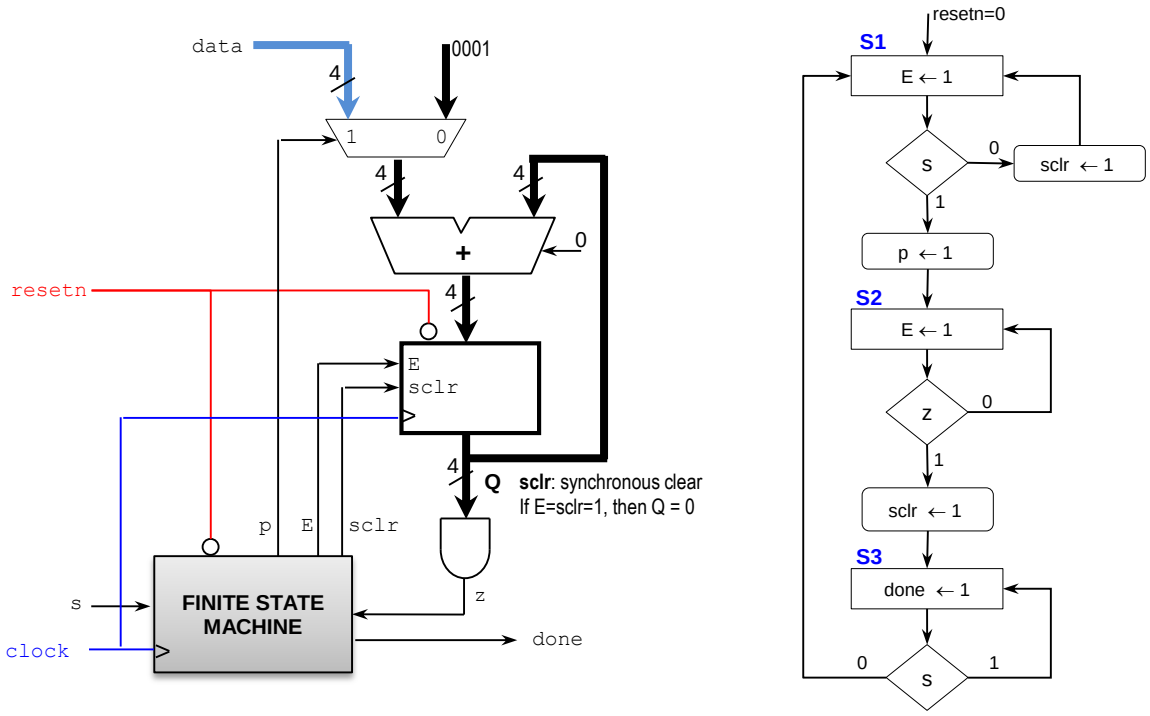
```
library ieee;
use ieee.std_logic_1164.all;

entity circ is
   port ( clk, resetn: in std_logic;
          r, p, q: in std_logic;
          x, w, z: out std_logic);
end circ;
```

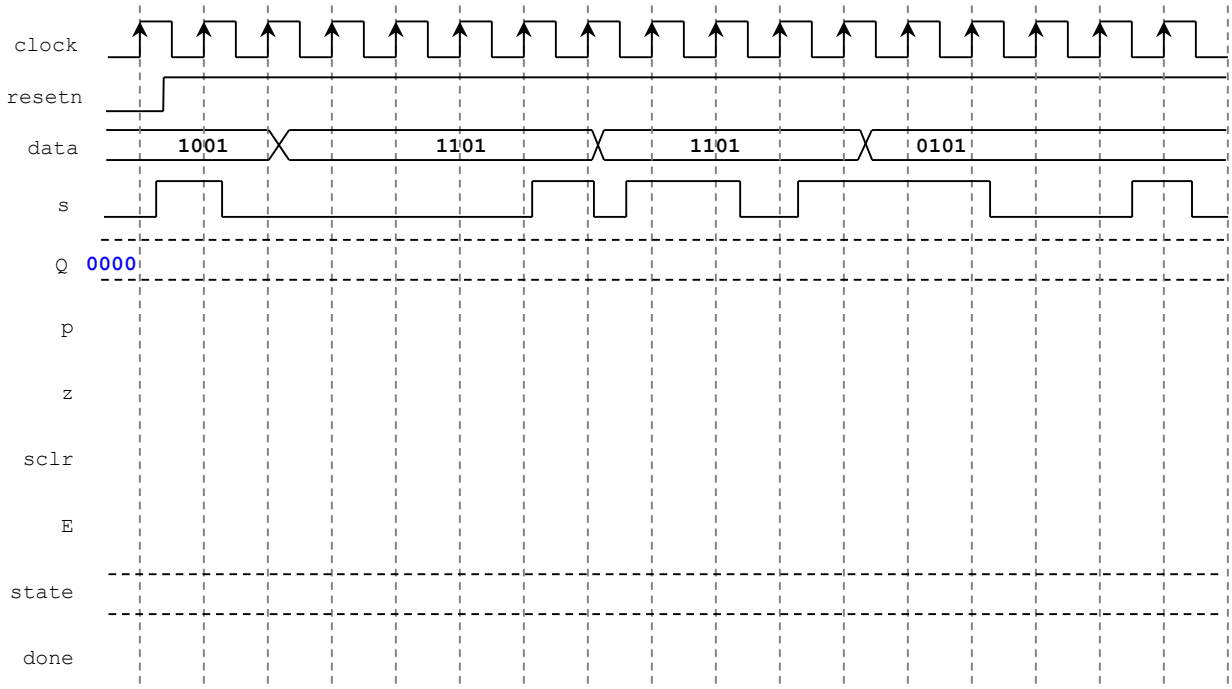
```
architecture behavioral of circ is
   type state is (S1, S2, S3);
   signal y: state;
begin
  Transitions: process (resetn, clk, r, p, q)
  begin
     if resetn = '0' then y <= S1;
     elsif (clk'event and clk = '1') then
        case y is
          when S1 =>
            if r = '1' then
               y <= S2;
            else
               if p = '1' then y <= S1; else y <= S3; end if;
            end if;

          when S2 =>
            if p = '1' then y <= S1; else y <= S3; end if;

          when S3 =>
            if q = '1' then y <= S3; else y <= S2; end if;

        end case;
     end if;
  end process;

  Outputs: process (y, r, p, q)
  begin
      x <= '0'; w <= '0'; z <= '0';
      case y is
         when S1 => if r = '0' then
                       if p = '1' then
                          w <= '1'; x <= '1';
                       end if;
                    end if;

         when S2 => if q = '0' then x <= '1'; end if;
                    if p = '0' then z <= '1'; end if;

         when S3 => if q = '0' then x <= '1'; end if;
      end case;
  end process;
end behavioral;
```



PROBLEM 5 (18 PTS)

- Complete the timing diagram of the following digital circuit that includes an FSM (in ASM form) and a datapath circuit.





PROBLEM 6 (15 PTS)

- Attach a printout of your Project Status Report (no more than three pages, single-spaced, 2 columns). This report should contain the current status of the project. You **MUST** use the provided template (`Final Project – Report Template.docx`).